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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/862,471	05/23/2001	Mitsuharu Kawaguchi	NU-01007	7469

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EXAMINER
TREAT, WILLIAM M

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 06/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Office Action Summary	Application No.	Applicant(s)
		09/862,471	KAWAGUCHI, MITSUHARU
		Examiner	Art Unit
		William M. Treat	2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _04 April 2005_.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-4 and 6-15_ is/are pending in the application.

     4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-4 and 6-15_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

     a)☒ All   b)☐ Some * c)☐ None of:

       1.☒ Certified copies of the priority documents have been received.

       2.☐ Certified copies of the priority documents have been received in Application No. _____.

       3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

     * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
     Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
     Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

1.   Claims 1-12 are presented for examination.

2.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3.   Claims 1-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Hunt

(Patent No. 5,740,391).

4.   Hunt taught the invention of exemplary claim 1 including an instruction buffer

(316) for a pipeline processor (310) comprising: a sequence of instructions arranged in

an order determined beforehand (col. 7, lines 25-67); a first buffer (342) including

entries arranged in a preselected entry number order for storing said sequence of

instructions; and a second buffer (344) including other entries for storing instructions,

wherein an instruction stored in any one of said other entries earlier than other

instructions is issued earlier than said other instructions, wherein any one instruction of

said sequence of instructions stored in any one of the entries of the first buffer

designated by a relatively lower entry number than another instruction in another entry

is prior, in order, to another instruction stored in another entry of the first buffer different

from the entry containing the one instruction designated by a relatively higher entry

number than said one instruction of said sequence of instructions: and wherein said first

and second buffers each issue instructions in storage entry order (col. 6, lines 52-62;

col. 7, lines 25-67; and Figs. 4(a-c)).

5.   As to claim 2, Hunt taught the instruction buffer as claimed in claim 1, wherein

the entries of the first buffer each show whether or not the instruction stored therein is

ready to be issued. At col. 7, lines 29-34, Hunt states: "In the preferred embodiment

system 300 of FIG. 3, the instruction buffer 316 is reordered by the hardware to

maximize pipeline efficiency such that instructions which are not waiting for a result from

prior instructions are launched for execution first." In the preferred embodiment the

order of each entry indicates whether or not the instruction stored in the entry is ready to

be issued.

6.   As to claim 6, Hunt taught a method of controlling a buffer queue for a pipeline

processor, comprising the steps of: generating a first group of instructions in a priority

order determined beforehand; generating a second group of instructions belonging to

said first group of instructions and capable of being executed; and executing one of said

second group of instructions highest in said order among said first group of instructions

(col. 6, lines 52-62; col. 7, lines 25-67; and Figs. 4(a-c)). Note, in particular, col. 7, lines

34-56.

7.   As to claim 7, Hunt taught the method as claimed in claim 6, further comprising

the steps of: generating a third group of instructions included in said first group of

instructions; and generating a fourth group of instructions included in said first group of

instructions and not dependent on said third group of instructions; wherein when one of

said fourth group of instructions highest in order does not belong to said second group

of instructions, none of said fourth group of instructions is executed. Note that in Figs. 3

and 4(a-c) Hunt has depicted a pipelined computer with an ALU unit and a memory

management unit with a FIFO instruction buffer for each unit which would result in issuing one instruction to each unit. Based on how Hunt describes the system of Figs. 4(a-c) (col. 7, lines 34-56) an instruction of the second group would issue before an instruction of the fourth group.

8.   As to claim 8, Hunt taught the method as claimed in claim 7, wherein one of two instructions belonging to said third group or fourth group of instructions is not executable until the other instruction of said two instructions is executed (col. 7, lines 42-54).

9.   As to claim 9, Hunt taught the method as claimed in claim 8, wherein the instructions belonging to said third group are executed at the same time as the instructions belonging to said fourth group (col. 7, lines 34-56).

10.   As to claim 10, Hunt taught the method as claimed in claim 9, wherein the instructions belonging to said third group and the instructions belonging to said fourth group are operation instructions and memory access instructions, respectively (col. 7, lines 54-56).

11.   As to claim 11, Hunt taught a buffer queue control for a pipeline processor comprising: a reorder buffer for registering a plurality of instructions in an order of instructions; a first buffer for storing first instructions included in the plurality of instructions; a second buffer for storing, among the plurality of instructions, second instruction other than the first instruction; said second instruction including an instruction that should be issued after said first instruction; said first buffer including a plurality of first entries for sequentially storing the first instructions in said order of instructions; said

buffer queue control further comprising: means for releasing any one of the plurality of

first entries that stores an instruction that issued; means for shifting any one of the first

instructions that is not issued to an entry prior, in order, by one; means for issuing one

of the second instructions, which can be issued, earliest in said order of instructions;

and means for deleting any one of the plurality of instructions that has been executed

and is earlier, in said order of instructions, than instructions not executed (col. 7, lines

34-56). Note that the pointer (PTR_EXECUTE of Figs. 4(a-c)) provides for a logical

shift of instructions by one as opposed to a physical shift by one. Since applicant does

not differentiate as to the type of shift, this is not a distinguishing point for applicant's

claims. And, were applicant to claim a physical shift the examiner would not consider

that to distinguish over other conventional instruction buffers which physically shift given

Hunt's statement that "the method of arbitrating for launching and method for launching

instructions for execution may be implemented using any workable scheme" (col. 7,

lines 34-36).

12.   As to claim 12, Hunt taught, the buffer queue control as claimed in claim 11

further comprising the means for issuing any one of the first instructions that is earliest

in said order of instructions and ready to be issued (col. 7, lines 24-56).

13.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

14.. Claims 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hunt (Patent No. 5,740,391).

15. As to claim 3, Hunt taught the instruction buffer as claimed in claim 2, wherein the instruction first issued is from among the entries of the first buffer whose instructions are ready to be issued (see paragraphs 4-5, *supra*). He did not specifically teach issuing "the entry having a lowest entry number among said entries of the first buffer whose instructions are ready to be issued"; however, the examiner takes Official Notice the method claimed is conventional. One of ordinary skill is motivated to use the method (i.e., issue the one having the lowest logical entry number among the instructions ready to be issued (i.e., the first one in program order)) because, to do otherwise, requires additional logic to track instructions passed over and, potentially, retards the instruction retirement process slowing overall processor performance.

16. As to claim 4, whether the entries of the first buffer storing the instructions are lower in logical or physical entry number order than the entries storing no instructions as in a circular buffer used as a queue (logical) or a queue which constantly shifts in new instructions at the top (physical), the examiner takes Official Notice of the fact both are conventional methods "for launching instructions for execution" (col. 7, line 35) and fall within the scope of Hunt's invention. One is motivated to use such conventional methods because they are well-known and readily implemented by one of ordinary skill.

17. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

18.   Claims 13-15 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

19.   In claims 13-15, applicant claims the second buffer has an issuance pointer and a head pointer. Applicant's drawings show the head pointer (56) associated with the reorder buffer (21) and only the issuance pointer (72) associated with the second instruction buffer (22). Applicant's original disclosure does not support applicant's claims 13-15 which represent new matter.

20.   The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

21.   Claims 13-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

22.   See paragraph 19, *supra*, for an explanation of the problem.

23.   Any inquiry concerning this communication should be directed to William M. Treat at telephone number (571) 272-4175. The examiner works at home on Wednesdays but may normally be reached on Wednesdays by leaving a voice message using his office phone number. The examiner also works a flexible schedule but may normally be reached in the afternoon and evening on three of the four remaining weekdays.

24.   Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

WILLIAM M. TREAT
PRIMARY EXAMINER